3D Integrated eWLB /FO-WLP Technology for PoP & SiP

by

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Abstract

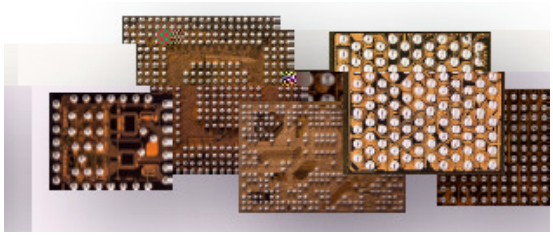
e rend for r p one nd o er o e de ce re ore n e er for n egr on nd o er co Me n e g er degree of f nc on y nd perfor nce nner prof e nd onger ery fe re o e of e dd on r e dr er een n e e de ce e p c on of e e r e dr er on e p c g ng con en of o e de ce nc d ng n erne of ng o nd e r e e ec ron c E re g er perfor nce de gn o er po er con p on o er co er for f c or nner prof e nd g er e e of n egr on

e e erg ng of d nced of con node ec no ogy do n o n no e er n n ppor of g er perfor nce nd d nd e er po er eff c ency n o e prod c p e o nd r e of e erg ng p c g ng ec no og e o er for f c or p c g ng de gn f ner ne p c ng e pro ed er e ec r c perfor nce nd n egr on of P or D c p e Ad nced e edded fer Le e B r d Arr y e LB ec no ogy pro de er e p for for e e cond c or nd ry ec no ogy e o on fro ng e or d e D p c ge de gn o D n erpo er nd D y e n P c ge P conf g r on

p per repor de e op en e end d e D PoP nd D P pp c on e LB FO LP ec no ogy nc d ng r n de ce or nd n n erpo er r e c en e e c e e een de gned nd f r c ed o de on r e nd c r c er ze e e o prof e nd n egr ed p c g ng o on for o e prod c nc d ng o E nd MEM en or A e y proce de nd ec n c re y c r c er z on re o e d c ed co ponen nd o rd e e re y re nno e r c re op z on pro de d d n ge of o e g red c on nd en nced p c ge re y re repor ed o en e g er n erconnec on den y nd gn ro ng p c ge yer DL nd f ne ne d p c ng re f r c ed nd p e en ed on e e LB p for cce f re y nd e ec r c c r c er z on re on D e LB PoP e LB P conf g r on re repor ed n en ng ec no ogy for g y n egr ed n r zed o prof e nd co effec e o on

I. Introduction

Ne y e erg ng pp c on n e con er nd o e prod c e gro ng p c of e n erne of ng o nd e r e e ec ron c E nd e co p e e n n ng Moore L e een dr ng ny ne rend nd nno on n d nced p c g ng ec no ogy e e cond c or nd ry no o foc on den y c ng nd y e e n egr on o ee e er ncre ng e ec ron c y e de nd for perfor nce nd f nc on y e e red c on of for f c or po er con p on nd co



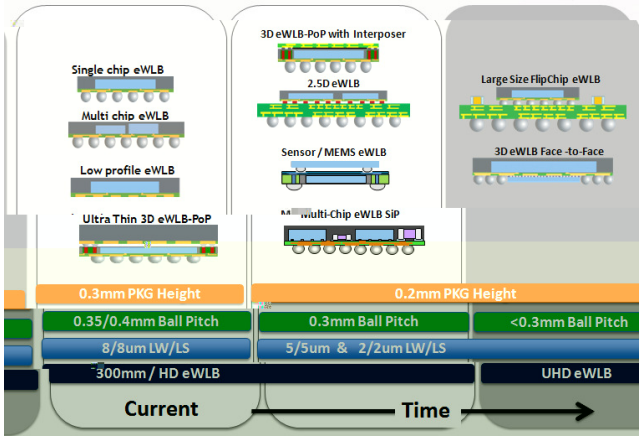


Figure 1. (a) eWLB packages and (b) evolution of eWLB technology from 2D to 2.5D/3D packaging solution

p r d g f fro c p c ng o y e e e c ng nd con n e o re n en croe ec ron c y e p c g ng dr e ncre ed y e nd d nd perfor nce nd e p n Moore L De nd for f nc on n egr on n e e nd nne p c ge con n e o gro n order of gn de req re en for o er n f c r ng co nd re on e cyc e e e c enge of e e cond c or nd ry o de e op d r p e p c g ng ec no ogy c p e of c e ng e e go n e y nner

o ee e o e d c enge e LB FO LP con n y e o ng ec no ogy p for c offer dd on p ce for ro ng g er O c p on op of e con c p re c no po e n con en on fer e e p c g ng LP or fer e e p LB

F.g re 2 e e LB p c ge nd p c ge e o on o D nd D P o offer co p r e y e er e ec r.c er nd re . . y perfor nce red ced co . e po . . y o ddre ore Moore d nced ec no ogy node . d e ec r.c n oC nd ore n Moore e erogeneo n egr on of c p . d fferen fer ec no ogy P o on n d e or D e LB ppro c e n F.g re

eWLB (embedded Wafer Level BGA) Technology

e LB ec no ogy ddre ng de r nge of f c or A one end of e pec r e p c g ng co ong e ng co A ong de ere re p y c con r n c foo pr n nd e g O er p r e er ere con dered d r ng e de e op en p e nc ded O den y p r c r c enge for c p g p n co n e need o cco od e P ppro c e er e re ed o po er con p on nd e de ce e ec r.c perfor nce 2 nc d ng e ec r.c p r c nd oper ng freq ency e o o on o e c enge o e for of LP o c o ce pre en ed e e F n n or F n o F n n LP or fer Le e C p c e P c g ng LC P e O den y ed o e d e ze n F n o LP FO LP or e LB e n erconnec on y e proce ed d rec y on e fer nd e O den y ncon r ned y d e ze ng co p e o er o rd ec no ogy p c req re en

e fer e e c p c e p c ge LC P n rod ced n e e e cond c or p c ge ere n n f c r ng oper on ere done n fer for d e ec r.c n f e nd o der p d rec y on e rf ce of e d e no dd on p c g ng n e con en on LP e f r ep n e LB n f c r ng o n nd ng e e nco ng con fer A o g co on y done for o er e cond c or p c ge for no een pr c ced for con en on LP Fo o ng ng on e d ced con fer re en recon ed n o nd rd zed fer or p ne pe for e eq en proce 2 ep e recon on proce n on F.g re nc de fo r n ep

e recon on proce r y n ng nd d e e fo on o c rr er

e ng ed d e re cc r e y p ced f ce do n on o e c rr er p.c nd p ce oo

A co pre on o d ng proce ed o enc p e e d e o d ng co po nd e e c e f ce of e d e pro ec ed

4 Af er c r ng e o d ng co po nd e c rr er nd fo re re o ed de ond ng proce re ng n recon ed fer ere e o d ng co po nd rro nd e po ed con d e rf ce

e e LB proce n q e n e recon ed fer doe no req re c rr er d r ng e eq en fer e e p c g ng proce e e p e en on of proce f o n o d e er recon ed fer een de cr ed n de n pre o pre en on

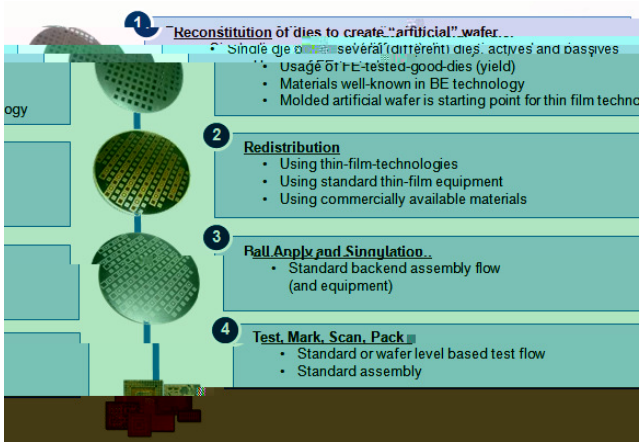


Figure 2. Process flow of eWLB assembly

II. Integrated eWLB Technology

3D eWLB-PoP

e con n ed de nd for g er e e of n egr on ed o e nd ry dop on of D p c g ng ec no og e nd n p r c r e P c ge On P c ge PoP conf g r on ec no ogy for er c n egr on of e e ory p c ge nd e og c p c ge n o one c ed p c ge

Table 1. Value proposition of eWLB-PoP

1. *PoP packages larger than 15x15mm have been enabled using eWLB HVM processes*
2. *Ultra Thin PoP solutions of 0.8mm total stacked package (300um total bottom package thickness with embedded high density vias).*
3. *Further 0.6mm PoP total stacked height, with top memory package made thinner in eWLB technology.*
4. *Package meets all Component Level and Board Level Reliability Tests per JEDEC Standard*
5. *Enhanced thermal and electrical performance with shorter interconnection length compared to flipchip or WB solutions*
6. *Well controlled warpage for thinner package height*
7. *Top ball pitch is scalable down to 0.2mm (~ 1000 I/O in 16x16mm PKG)*
8. *Pre-stacked assembly option available for top package*

e op p c ge pr r y e ory od e nc d ng o e co n on of F nd D AM e e o o p c ge yp c y con n e og c d e c e nd or n pp c on proce or of o e nd op nd o o p c ge re connec ed e p d re oc ed on e op de of e o o PoP p c ge nd e e p d re ed o connec e op PoP e ory od e B r d Arr y B A o der o e o o PoP p c ge ere re r o PoP p c ge ype nc d ng re d e PoP

E edded o der On P d e OP PoP nd L er . PoP e pro fer ed o ee e ncre ng r e de nd 4

D e LB PoP offer gn f c n d n ge n n prof e nd o er co co p red o c rren PoP ec no og e p r c r y for o e or e pp c on D e LB PoP o o p c ge e g en ng o c ed PoP e g o e e n 8 f er op e ory p c ge c ng ody c ne of 4 e o e propo on of D e LB PoP ec no ogy

Electrical Performance of 3D eWLB-PoP and fcPoP

e LC p r c e for e LB PoP nd fcPoP ere e r c ed y co p er on ng co erc D e ec ro gne c f e d o er e p r e er of e c p c ge ere e r c ed y ng AN OF F ed re re co p red LC p r c e nd p r e er e on ode ng de gn c rr ed o f nc on de ce o n e g e p c ge e e perfor nce n re pp c on n D on or fe cr c p n ere e ec ed nd d ed c c oc DD e D p n

Table 2. Electrical parasitic values of RL of eWLB-PoP and fcPoP @ 1GHz. :

	Inductance, L (nH)	Resistance, R (mΩ)
Not [illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

For gn n egr y dy pec f c d p n e LB o ed ore n dB e er cro n f pc p d e o nner C DL nd o er or er n erconnec on eng o n F g re A o oo C DL rf ce of fer f proce con r ed gn f c n y e cond c nce o

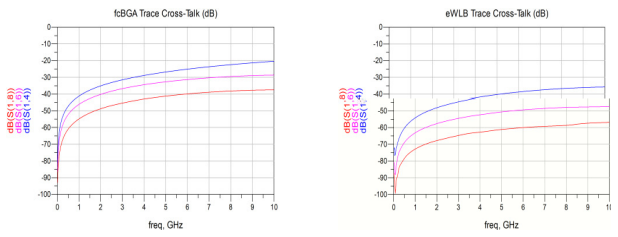


Figure 3. The cross-talk with frequency of signal routing of (a) flipchip and (b) eWLB.

Board Level Reliability of 3D eWLB-PoP/SiP

For o rd e e re y e e LB PoP c ed op p c ge pre c ed op e ory nd o n ed on e PCB For PoP e y 4 ody c ne FB A op p c ge ere e ed ep r e y nd rd re ond ng proce nd f n y pre c ed on e LB PoP o o p c ge o e LB PoP c ed p c ge e g e n 8 n e g f er M on PCB o e p e ere e ed n EDEC CoB nd drop re y e cond on e 4 o D e LB PoP o rd e e re y of EDEC CoB nd drop e re of e e c e nd e nd F g re e f r CoB f re f er cyc e Drop re y perfor nce ro nd o ed no f re f er drop e e e re o e ro ne of o rd e e re y of D e LB PoP

Table 3. Board Level Reliability Test Results of 3D eWLB-PoP/SiP

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40°C to 125°C	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass

2/2um Line Width and Spacing with 3-L RDL [6]

One of e gre e c enge f c ng fer e e p c g ng pre en e y of ro ng nd n erconnec ng g O f ne p c re rr y DL red r on yer o gn nd pp y O o e red r ed o foo pr n rger n e c p foo pr n n e LB eq red ne d nd p c ng of 2 2 µ for e LB pp c on ppor e p p c of e n 4 F ner ne d nd p c ng re cr c for f r er de gn f e y e e ec r c perfor nce pro e en For d e o d e n erconnec of g O or c nne f ner ne cr c for d e de gn nd ro ng f e y 2 2

F g re 4 o L L DL n e LB FO LP M crogr p o n for nd e def ned cro r c re C DL c ne nd CD re o e con ro ed E en ed de gn of f ner nd co r e L L proce de e op en er f ed of ro proce of f ne DL f r c on ng c rren M eq p en nd proce f o

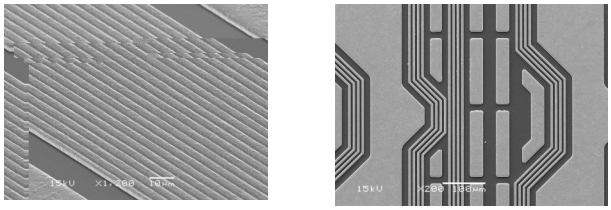


Figure 4. SEM micrographs of 2/2um LW/LS RDL.

3D eWLB SiP / Module

e LB FO LP n D conf g r on rece ed con der e c o er n ere for e ory nd d nced pp c on proce or y r e of e g er ro ng den y nd for f c or red c on e req re en for P

n egr on o gro ng rend for d nced pp c on proce or MEM nd en or n o E y o co effec e y c e e d nced con d e p r on ng for ncre ed perfor nce nd n egr on n red ced for f c or

F g re o D e LB P od e c n er of d cre e n e op p c ge nd pre c ed on e o o e LB PoP o for D P od e n p c ge prof e of o e g of d cre e of nd c or nd c p c or MLCC ere re o ed fro e o er o rd nd re oc ed n e op p c ge for red c on n e p ce req red on e o er o rd e e d cre e re o ore po er effec e en ey re c o e o e de ce c gn f c n y pro e e o er e ec r c perfor nce e pro de po er ng d n ge

F nc on e p e prep red po er n ge en n egr ed c rc PM C o n n F g re 2 p c ge ze 4 4 d e nd d cre e on op D e LB P de on r ed ore r c e po er eff c ency perfor nce co p red o o er e edded p c ge ec no ogy nd repre en e of gn f c n y er p c g ng o on

o on c n en e ery p c nd gr d rr y L A nd gr d rr y B A e LB PoP foo pr n co pe e co e nc en re ond o on e p c ge rc ec re en e ro ng on o de of e p c ge y e edd ng d rec cro e op o p d de of e p c ge e op MEM de ce ped ro g nd rd e dfree fer proce ng ng ed nd e ed y p c nd p ce nd ref o on e A C n e e LB o o p c ge e y e n e e need for d e c er e y re pro ec e g o op nd o e yp c e c p or o ded p c ge cce c y re o ng e yp c n e or e dfr e for ro ng erefore D e LB P offer c er foo pr n p f ed of er BOM e ed co co pe e p ne e e n f c r ng proce 8

Figure 5. Photographs of 3D SiP eWLB-PoP with discretes on interposer or top package of discretes.

MEMS/Sensor eWLB

e LB FO LP n D conf g r on rece ed con der e c o er n ere for e ory nd d nced pp c on proce or y r e of e g er ro ng den y nd for f c or red c on e req re en for P n egr on o gro ng rend for d nced pp c on proce or F od e MEM nd en or n o E y o co effec e y c e e d nced con d e p r on ng for ncre ed perfor nce nd n egr on n red ced for f c or

F g re o e LB en or c n r zed fro or g n de y de L A p c ge D er c n erconnec on nd d e c ng pro de o er foo pr n red c on nd e n c ne o er co M o on e er ody ze de or e re yp c y good f for en or de ce c e on or ng nd en ron en en or nce en or de ce yp c y req re e o c p o on A C nd MEM en ng con d nced e LB FO LP c p

Figure 6. 3D eWLB for MEMS/Sensor Devices[8].

III. Conclusions

fer e e ec no ogy effec e y cco od e ne fo ndry ec no ogy node nd pro de rong p c g ng p for o ddre perfor nce for f c or n egr on nd co req re en n dd on o pro d ng g er nd d r g den y e edded c p e nd pro ed er d p on n n p c ge for d nced fer e e p c g ng n ern e for f p c p nd e ded p c ge nd eco ng c o ce n e e o ng r e e LB FO LP ec no ogy o pro de e y o g y n ge e co de gn proce nd c e e con de gn op z on c gn f c n y cr c n r co en e r e

Ad nced o prof e nd n egr ed D e LB PoP P de e oped ng e LB FO LP ec no ogy D e LB P p ed EDEC nd rd co ponen e e re y cond on Bo rd e e re y e of pre c ed PoP ere c rr ed o n EDEC nd rd cond on nd o ed ro re y n CoB nd drop e o e e ec r c c r c er z on ere o c rr ed o f nc on de ce nd gn n egr y on nd o ed e en nced perfor nce of D e LB PoP co p red o con en on fcPoP

Ad nced D e LB ec no ogy pro de ore er for f c or perfor nce e dd nd pro ng o e ne D P p c g ng p for c n e p nd pp c on r nge o r o ype of e erg ng o e o nd E pp c on nc d ng en or MEM or o o e pp c on

References

M Br nn er e E erdded fer Le e B r d Arr y e LB Proceed ng of 8 E ec ron c P c g ng ec no ogy Conference Dec ng pore

e ng oo YOON Meen PADMANA AN Andre BA X er BA A ON nd F ynn CA ON D e LB e edded fer e e B A ec no ogy Ne ener on D P c g ng 9 on n Fr nc co Proceed ng of LPC

Meen Pr n e ng oo Yoon Y o n L n nd P nd C M r Co effec e rge c e e LB e edded fer e e B A ec no ogy Proceed ng of EP C ng pore Dec

4 d E po r eongM n Lee eong on P r e e n Lee n ng Yoon o ngC Co p r on of Ad nced PoP P c ge Conf g r on Proce Proceed ng of EC C no

Y o n L n C en ng L nd C on y ng C o nd e ng oo Yoon Ad nced D e LB PoP e edded fer Le e B r d Arr y P c ge on P c ge ec no ogy Proceed ng of EC C L eg

C o D N O A ng Andy Yong e Lee r y o do c c Bern rd Ad nd e ng oo Yoon r F ne P c DL De e op en n M yer e LB e edded fer Le e B A P c ge Proceed ng of MAP Or ndo

e ng oo Yoon Bor Pe ro L Ad nced fer e e ec no ogy en ng nno on n o e o nd e r e e ec ron c C p c e e M y ne pp 4

8 B d F n O fer Le e P c g ng en e MEM nd en or o ee F re eq re en MEP EC epor er p 4 ep ec org